EXHIBIT 1

1   Vol. 2, Pgs. 1-239

2   Exhibits See index

3

4   UNITED STATES DISTRICT COURT

5   FOR THE DISTRICT OF DELAWARE

6

7   - - - - - - - - - - - - - - - - - - -

8   POWER INTEGRATIONS, INC., a Delaware

9   corporation

10   Plaintiff

11   v.   CA No. 04-1371

12   FAIRCHILD SEMICONDUCTOR

13   INTERNATIONAL, INC., a Delaware

14   corporation, and FAIRCHILD SEMICONDUCTOR

15   CORPORATION, a Delaware corporation

16   Defendants

17   - - - - - - - - - - - - - - - - - - -

18   CONTINUED DEPOSITION of PAUL HOROWITZ, Ph.D.

19   Tuesday, January 30, 2007 - 9:36 a.m.

20   Fish & Richardson P.C.

21   225 Franklin Street

22   Boston, Massachusetts

23

24   - - - - - Jill K. Ruggieri, RMR/CRR - - - - -

25

1   And if someone said have you

2   modulated your oscillator about a target

3   frequency, the answer would be, sure, the

4   central frequency of the band would be --

5   could be called a target frequency.

6   It's analogous language.

7   Q   Okay.

8   I think that that seems to be a

9   backwards perspective.

10   Are you saying that, well, any time

11   you do spread spectrum you're going to get

12   an average frequency somewhere in the range,

13   and therefore, you would construe that to be

14   the target frequency?

15   A   Well, average -- you're going to get some

16   spectrum. And the spectrum has some center,

17   and if the modulation is -- if you -- if

18   you --

19   There's several different ways one

20   might produce such a set of frequencies.

21   One might use a direct digital synthesis

22   producing each frequency in isolation or,

23   alternatively, and in the prior art that's

24   being talked about here, one would achieve

25   it by using a voltage-controlled oscillator

1   or ramp-controlled oscillator whose

2   frequency variation can be thought of as

3   deviation from a central frequency.

4   And in that particular kind of

5   application, the use of the term "central

6   frequency" or "unmodulated frequency" or

7   "target frequency" would be synonymous or

8   nearly synonymous.

9   Q   So is it your opinion, then, that any time

10   you modulated the frequency of an

11   oscillator, which would have by its nature a

12   base frequency, an unmodulated frequency,

13   that then you would be varying about a

14   target frequency in that case?

15   A   I think it -- certainly in the form of a VCO

16   whose control signal deviates about --

17   deviates from its unmodulated frequency,

18   that it would be reasonable to use the term

19   "target frequency" as the central band of

20   the modulated frequencies.

21   I think it depends a little bit on

22   context, and I would like to see the context

23   in this case. Give me a moment here. We're

24   still talking about this --

25   Well, we're talking about the '876

1   patent, and we're talking about the Markman

2   interpretation?

3   Q   Correct.

4   (Witness read document.)

5   A   In the context of the '876 patent -- and

6   it's Markman -- frequency jittering means

7   varying the switching frequency of an SMPS

8   about a target frequency to reduce EMI.

9   The -- my understanding, and one of

10   skill in the art's understanding, would be,

11   would have been, that the switching supply

12   absent the modulation would operate at some

13   frequency.

14   That would be the target frequency of

15   this interpretation, that the addition of

16   modulating circuitry causes the frequency to

17   vary about that frequency.

18   That would be the same frequency that

19   I've described earlier today as the central

20   frequency or the middle of the spectrum or

21   the center of the band.

22 Q   What if the modulation was all additive,

23   meaning that it only modulated above the

24   base frequency?

25 A   Well, you could do that.

EXHIBIT 2

```
 1              IN THE UNITED STATES DISTRICT COURT

 2                  FOR THE DISTRICT OF DELAWARE

 3                           --oOo--

 4

 5    POWER INTEGRATIONS, INC.,

      a Delaware corporation,

 6

 7           Plaintiff,

 8    vs.                            Case No. 04-1371 (JJF)

 9    FAIRCHILD SEMICONDUCTOR

      INTERNATIONAL, INC., a

10    Delaware corporation, and

      FAIRCHILD SEMICONDUCTOR

11    CORPORATION, a Delaware

      corporation,

12

13           Defendants.

14    _____//

15    Pages 1 through 243 inclusive.

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18

19             DEPOSITION OF ROBERT BLAUSCHILD

20                    March 9, 2007

21                     VOLUME II

22

23

24    REPORTED BY:

25    TRACY FLETCHER, CSR NO. 11683
```

1	discussions you had yesterday to prepare for your	01:15
2	deposition?	01:15
3	A. No.	01:15
4	Q. Do you recall any specifics of the discussion	01:15
5	you had with Mr. Headley or Mr. Pollack yesterday?	01:15
6	A. Any specifics? Yes.	01:15
7	Q. What do you recall?	01:15
8	A. Specifically -- let's see, we talked about --	01:15
9	well, it's just talking about the stuff that was in my	01:15
10	report, the specific, um, disagreements I had with Dr.	01:15
11	Horowitz. Um, we talked -- I'm sorry, we talked about,	01:15
12	um, target frequencies. That's what I can remember. I	01:16
13	know we talked about lots of stuff that was in my	01:16
14	report.	01:16
15	Q. What did you discuss concerning target	01:16
16	frequencies?	01:16
17	A. The lack thereof in the three -- the '876	01:16
18	references, um, Habetler, Wang and Martin.	01:16
19	Q. Do you believe that it's required that a	01:16
20	reference disclose a target frequency in order to meet	01:16
21	the elements of the '876 patent?	01:17
22	MR. POLLACK: Objection. Vague and ambiguous.	01:17
23	THE WITNESS: Disclose a target frequency, um,	01:17
24	you don't -- can I check the claim construction?	01:17
25		

1   MR. DE BLANK: 01:17

2   Q.   Of course.   01:17

3   A.   I want to see something. I can get it out of   01:17

4   my report.   01:17

5   Q.   If it's in your report, that's fine. If you'd   01:17

6   like I have a copy of the court's actual --   01:17

7   A.   I think it's in my report, that's why I wanted   01:18

8   to look. Um, I believe it doesn't have to say the   01:18

9   target frequency is hundred kilohertz, and we're going   01:18

10   to vary about that. It doesn't have to say that. It   01:18

11   doesn't have to have a specific one. It could say we   01:19

12   have this frequency, and we're going to vary about that,   01:19

13   and that could be -- depending on how the wording was,   01:19

14   that could be the target frequency. You don't have to   01:19

15   give it a spec, for example.   01:19

16   Q.   Okay. But it's your opinion that a target --   01:19

17   that a target frequency is required to practice Claim 1   01:19

18   of the '876 patent?   01:19

19   A.   Uh-huh. I believe you have to vary around --   01:19

20   in a range around the target frequency, yes.   01:19

21   Q.   And you believe that Fairchild would not have   01:19

22   met its burden of proof to show that a reference   01:19

23   anticipates Claim 1 of the '876 patent without proving   01:20

24   that the reference varies the frequency around a target   01:20

25   frequency?   01:20

1   MR. POLLACK: Objection.   01:20

2   THE WITNESS: I would say if it doesn't vary   01:20

3   around the target frequency, it's not -- let me look   01:20

4   again. I think it's -- then I would say it's not the   01:20

5   frequency jittering circuit as defined by the court.   01:20

6   Yeah. I think that's right.   01:21

7   MR. DE BLANK: 01:21

8   Q.   So you believe it's Fairchild's burden to prove 01:21

9   that a reference varies the oscillator frequency around 01:21

10   a target frequency in order to show that that reference 01:21

11   meets each element of Claim 1 of the '876 patent?   01:21

12   MR. POLLACK: Objection. Vague and ambiguous.   01:21

13   THE WITNESS: I believe that Claim 1 -- yep. I   01:21

14   believe that Claim 1 requires a frequency jittering   01:21

15   circuit, and the court construed that to require varying 01:22

16   about a target frequency.   01:22

17   MR. DE BLANK: 01:22

18   Q.   We were discussing the, um, preparation you had 01:22

19   with Mr. Pollack and Mr. Headley before today's   01:22

20   deposition. Other than the discussions concerning the   01:22

21   target frequency, are you aware -- can you recall any   01:22

22   other specific, um, topics you discussed with either   01:22

23   gentleman?   01:22

24   A.   We discussed single-ramp versus repeating   01:22

25   frequency variation circuit waveforms, and I can't   01:22

1	remember now if we discussed every reference with	01:22
2	respect to that or every one of Dr. Horowitz's opinions,	01:22
3	um, that was one of the topics. Um, just generally went	01:23
4	over each -- I can't even say that we went over each of	01:23
5	the seven circuit references versus what's in my report.	01:23
6	I'm trying to think of other topics of discussion. Um,	01:23
7	internal with respect to frequency variation signal.	01:23
8	Q. Is there anything about your supplemental	01:23
9	report, Exhibit 10, that you believe is inaccurate or	01:24
10	incorrect, or an opinion you would like to change?	01:24
11	MR. POLLACK: Objection. Compound, asked and	01:24
12	answered.	01:24
13	THE WITNESS: Not at this time. I think it's	01:24
14	correct.	01:24
15	MR. DE BLANK:	01:24
16	Q. Other -- other than the meeting you had with	01:24
17	Mr. Pollack and Mr. Headley yesterday, did you do	01:24
18	anything else to prepare for today's deposition?	01:24
19	MR. POLLACK: Objection. Asked and answered.	01:24
20	THE WITNESS: I read my report. I read my	01:24
21	prior deposition. I read the Habetler reference in part	01:24
22	again.	01:24
23	MR. DE BLANK:	01:25
24	Q. Other than the discussions you had with Mr.	01:25
25	Pollack and Mr. Headley yesterday, did you have any	01:25

EXHIBIT 3

1   IN THE UNITED STATES DISTRICT COURT

2   FOR THE DISTRICT OF DELAWARE

3   --oOo--

4

5   POWER INTEGRATIONS, INC.,

      a Delaware corporation,

6

7   Plaintiff,

8   vs.   Case No. 04-1371 (JJF)

9   FAIRCHILD SEMICONDUCTOR

      INTERNATIONAL, INC., a

10   Delaware corporation, and

      FAIRCHILD SEMICONDUCTOR

11   CORPORATION, a Delaware

      corporation,

12

13   Defendants.

14   _____//

15   Pages 1 through 243 inclusive.

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18

19   DEPOSITION OF ROBERT BLAUSCHILD

20   March 9, 2007

21   VOLUME II

22

23

24   REPORTED BY:

25   TRACY FLETCHER, CSR NO. 11683

1	Q. -- the switching frequency of the oscillator	02:49
2	shown in figure 1 of the Martin patent would vary about	02:49
3	a frequency or a set of frequencies, correct?	02:49
4	MR. POLLACK: Objection. Compound, lacks	02:50
5	foundation, vague and ambiguous.	02:50
6	THE WITNESS: Okay. Again, what's the	02:50
7	programming? Um, let's assume a whole bunch of	02:50
8	different codes in there. Is that what you're --	02:50
9	MR. DE BLANK:	02:50
10	Q. That's fine. So we'll assume that the contents	02:50
11	of the EPROM were programmed by drawing numbers out of a	02:50
12	hat; the contents were --	02:50
13	A. Big hat.	02:50
14	Q. Big hat. Programmed randomly, but they are not	02:50
15	programmed and set, and we are assuming that they're not	02:50
16	being reprogrammed during the operation of the Martin	02:50
17	circuit. Given that, isn't it true that there is --	02:50
18	that the oscillation -- sorry -- that the frequency of	02:50
19	the oscillator in figure 1 of the Martin patent varies	02:50
20	around a target frequency?	02:51
21	A. No. You didn't -- your design process did not	02:51
22	put into the hat saying this is my target, vary around	02:51
23	this. That was not in there.	02:51
24	Q. I understand. So you're saying that target --	02:51
25	the inclusion of the word target frequency requires an	02:51

1	intent by someone that it vary around a specific	02:51
2	frequency?	02:51
3	A. Yeah. That's -- that's my understanding of the	02:51
4	process.	02:51
5	Q. Okay. Would the device -- or the circuit shown	02:51
6	in figure 1 of the Martin patent work if the oscillator	02:51
7	were allowed to vary in frequency between zero and a	02:51
8	billion hertz?	02:51
9	A. By work --	02:51
10	Q. Well, let me --	02:51
11	A. Okay.	02:51
12	Q. Let me try it this way. A	02:51
13	voltage-controlled -- sorry. Figure 1 of the Martin	02:52
14	patent shows a voltage-controlled oscillator.	02:52
15	Voltage-controlled oscillators vary the frequency of the	02:52
16	oscillator based on the voltage received at the control	02:52
17	input, correct?	02:52
18	A. High level, yes.	02:52
19	Q. Good. The voltage-controlled oscillator can	02:52
20	vary a -- receive a range of frequencies at the control	02:52
21	input, correct?	02:52
22	MR. POLLACK: Objection.	02:52
23	THE WITNESS: Arrange a frequency --	02:52
24	MR. DE BLANK:	02:52
25	Q. Sorry, that was poorly phrased. A	02:52

EXHIBIT 4

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1              IN THE UNITED STATES DISTRICT COURT

2                 FOR THE DISTRICT OF DELAWARE

3                          --oOo--

4

5     POWER INTEGRATIONS, INC.,

      a Delaware corporation,

6

7           Plaintiff,

8     vs.                              Case No. 04-1371 (JJF)

9     FAIRCHILD SEMICONDUCTOR

      INTERNATIONAL, INC., a

10    Delaware corporation, and

      FAIRCHILD SEMICONDUCTOR

11    CORPORATION, a Delaware

      corporation,

12

13          Defendants.

14    _____//

15    Pages 1 through 243 inclusive.

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18

19           DEPOSITION OF ROBERT BLAUSCHILD

20                  March 9, 2007

21                    VOLUME II

22

23

24    REPORTED BY:

25    TRACY FLETCHER, CSR NO. 11683
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1	THE VIDEOGRAPHER: Back on the record. The	02:37
2	time is 2:37 p.m.	02:37
3	MR. DE BLANK:	02:37
4	Q. Mr. Blauschild, the term "frequency generator"	02:37
5	is being construed to mean varying the switching	02:37
6	frequency of a switch mode power supply about a target	02:37
7	frequency in order to reduce electromagnetic	02:37
8	interference; do you understand that?	02:37
9	A. Yes.	02:37
10	Q. This is a term, "frequency jittering," that	02:37
11	appears in what's called a preamble of the claim; do you	02:37
12	know what a preamble --	02:37
13	A. I do.	02:38
14	Q. Is it your opinion that the preamble to Claim 1	02:38
15	of the '876 is a limitation?	02:38
16	MR. POLLACK: Objection. Calls for a legal	02:38
17	conclusion, one that's already been decided.	02:38
18	THE WITNESS: Well, I agree with him in that	02:38
19	I'm not a lawyer, but my assumption was it was because	02:38
20	it was a construed term.	02:38
21	MR. DE BLANK:	02:38
22	Q. Okay. So it's your understanding that in order	02:38
23	to determine whether a circuit meets the elements of	02:38
24	Claim 1 of the '876 patent, it requires the oscillator,	02:38
25	the digital to analog converter, the counter elements as	02:38

1   set forth in Claim 1, but also that it vary the   02:38

2   switching frequency of a switch mode power supply about   02:38

3   a target frequency in order to reduce electromagnetic   02:38

4   interference; is that correct?   02:38

5   MR. POLLACK: Objection. Asked and answered.   02:38

6   THE WITNESS: I believe so. I had the wrong   02:39

7   patent in front of me, but it didn't make much sense. I 02:39

8   think so, yes.   02:39

9   MR. DE BLANK: 02:39

10   Q.   What is a target frequency as that term is used 02:39

11   in the -- in terms of frequency jittering?   02:39

12   A.   What my understanding of that is is you pick a 02:39

13   frequency, and this is based on what people do, you pick 02:39

14   a frequency, and then you wiggle around that frequency,   02:39

15   and it's the frequency you would have without the   02:39

16   wiggle.   02:39

17   Q.   So it's the frequency of the oscillator if   02:39

18   there were no frequency variation circuitry involved?   02:39

19   MR. POLLACK: Objection. Vague and ambiguous. 02:40

20   THE WITNESS: That's -- we're talking about two 02:40

21   different things. One is designing an oscillator that   02:40

22   has frequency jitter, and you design it by having a   02:40

23   target, and then you vary around it. The other one   02:40

24   doesn't have frequency jitter. You could have some   02:40

25   design value, um, whether you call that the target   02:40

1	frequency or not, it doesn't really apply because we're	02:40
2	not talking about that with respect to the claim	02:40
3	construction. Is that clear?	02:40
4	Q. I'm not sure I understand the last part when	02:40
5	you're saying whether you call it a target frequency	02:40
6	doesn't apply?	02:40
7	A. It's different. It's not the same kind of	02:40
8	design where you're designing a frequency jittering	02:41
9	circuit, and you have a target frequency, and then you	02:41
10	wiggle around that versus not -- totally different	02:41
11	design process.	02:41
12	Q. Okay. Maybe it would help me to understand if	02:41
13	you could tell me what the target frequency of figure 1	02:41
14	of the '876 patent would be?	02:41
15	A. My understanding of the target frequency would	02:41
16	be you could pick either the code of 0111 or the 100	02:41
17	code, either of those would be the target frequency, and	02:41
18	then you wiggle around that.	02:41
19	Q. I'm sorry. You were referring to figure 2 of	02:41
20	the --	02:41
21	A. Figure 2, yeah.	02:42
22	Q. And you're saying the target frequency is	02:42
23	either 0111 or 1110?	02:42
24	A. Yeah.	02:42
25	Q. Okay. Does --	02:42

EXHIBIT 5

```
1                IN THE UNITED STATES DISTRICT COURT

2                   FOR THE DISTRICT OF DELAWARE

3                             --oOo--

4

5    POWER INTEGRATIONS, INC.,

     a Delaware corporation,

6

7            Plaintiff,

8    vs.                            Case No. 04-1371 (JJF)

9    FAIRCHILD SEMICONDUCTOR

     INTERNATIONAL, INC., a

10   Delaware corporation, and

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11   CORPORATION, a Delaware

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13           Defendants.

14   _____//

15   Pages 1 through 243 inclusive.

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18

19            DEPOSITION OF ROBERT BLAUSCHILD

20                    March 9, 2007

21                     VOLUME II

22

23

24   REPORTED BY:

25   TRACY FLETCHER, CSR NO. 11683
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1	MR. DE BLANK:	01:17
2	Q. Of course.	01:17
3	A. I want to see something. I can get it out of	01:17
4	my report.	01:17
5	Q. If it's in your report, that's fine. If you'd	01:17
6	like I have a copy of the court's actual --	01:17
7	A. I think it's in my report, that's why I wanted	01:18
8	to look. Um, I believe it doesn't have to say the	01:18
9	target frequency is hundred kilohertz, and we're going	01:18
10	to vary about that. It doesn't have to say that. It	01:18
11	doesn't have to have a specific one. It could say we	01:19
12	have this frequency, and we're going to vary about that,	01:19
13	and that could be -- depending on how the wording was,	01:19
14	that could be the target frequency. You don't have to	01:19
15	give it a spec, for example.	01:19
16	Q. Okay. But it's your opinion that a target --	01:19
17	that a target frequency is required to practice Claim 1	01:19
18	of the '876 patent?	01:19
19	A. Uh-huh. I believe you have to vary around --	01:19
20	in a range around the target frequency, yes.	01:19
21	Q. And you believe that Fairchild would not have	01:19
22	met its burden of proof to show that a reference	01:19
23	anticipates Claim 1 of the '876 patent without proving	01:20
24	that the reference varies the frequency around a target	01:20
25	frequency?	01:20

1	MR. POLLACK: Objection.	01:20
2	THE WITNESS: I would say if it doesn't vary	01:20
3	around the target frequency, it's not -- let me look	01:20
4	again. I think it's -- then I would say it's not the	01:20
5	frequency jittering circuit as defined by the court.	01:20
6	Yeah. I think that's right.	01:21
7	MR. DE BLANK:	01:21
8	Q. So you believe it's Fairchild's burden to prove	01:21
9	that a reference varies the oscillator frequency around	01:21
10	a target frequency in order to show that that reference	01:21
11	meets each element of Claim 1 of the '876 patent?	01:21
12	MR. POLLACK: Objection. Vague and ambiguous.	01:21
13	THE WITNESS: I believe that Claim 1 -- yep. I	01:21
14	believe that Claim 1 requires a frequency jittering	01:21
15	circuit, and the court construed that to require varying	01:22
16	about a target frequency.	01:22
17	MR. DE BLANK:	01:22
18	Q. We were discussing the, um, preparation you had	01:22
19	with Mr. Pollack and Mr. Headley before today's	01:22
20	deposition. Other than the discussions concerning the	01:22
21	target frequency, are you aware -- can you recall any	01:22
22	other specific, um, topics you discussed with either	01:22
23	gentleman?	01:22
24	A. We discussed single-ramp versus repeating	01:22
25	frequency variation circuit waveforms, and I can't	01:22

1	does.	03:02
2	MR. DE BLANK:	03:02
3	Q. And if you turn to the page ending in 1863,	03:02
4	it's about five pages from the front.	03:03
5	A. Okay.	03:03
6	Q. At the end of the second column in the	03:03
7	beginning of the -- sorry -- end of the first column and	03:03
8	beginning of the second, Wang wrote, "For our purposes,	03:03
9	the programmed PWM waveform must meet several	03:03
10	constraints, both in the time and frequency domains."	03:03
11	Do you see where I'm reading on the bottom of the first	03:03
12	column?	03:03
13	A. Yes.	03:03
14	Q. And then he lists four constraints. C1, 2, 3	03:03
15	and 4 on the second column, correct?	03:03
16	A. Yes.	03:03
17	Q. Okay. The first constraint is that "The	03:03
18	programmed PWM waveform must have the same average	03:03
19	period and the same average duty cycle as the original	03:03
20	PWM waveform," correct?	03:03
21	A. That's what it says.	03:03
22	Q. So the Wang article teaches or states that	03:03
23	notwithstanding the frequency variation, the programmed	03:04
24	PWM waveform must have the same average period and same	03:04
25	average duty cycle as the original PWM waveform without	03:04

173

1	frequency variation, correct?	03:04
2	A. You lost me in the beginning of that question.	03:04
3	Q. Sure. I'm just confirming my understanding	03:04
4	that when it's distinguishing between the programmed PWM	03:04
5	waveform and the original PWM waveform in constraint C1,	03:04
6	that it's referring to -- the programmed PWM waveform is	03:04
7	the waveform with frequency modulation, and the original	03:04
8	PWM waveform is the waveform without frequency	03:04
9	modulation?	03:04
10	MR. POLLACK: Objection. Vague and ambiguous,	03:04
11	lacks foundation.	03:04
12	THE WITNESS: Okay. Frequency modulation,	03:04
13	again, I think that was -- we can look again, but I	03:04
14	think that specific term was included somewhere by the	03:05
15	court. If we're just using modulation to mean change,	03:05
16	then I'll agree with that, but as you know from my	03:05
17	report I don't think this has the -- the frequency	03:05
18	jittering of the patent.	03:05
19	MR. DE BLANK:	03:05
20	Q. You're referring to the -- again --	03:05
21	A. The Wang.	03:05
22	Q. -- to the preamble of Claim 1 --	03:05
23	A. Yeah.	03:05
24	Q. -- of the '876 patent specifically?	03:05
25	A. Yes.	03:05

1   Q.   And just to confirm again, it's your belief   03:05

2   that the Wang reference doesn't teach a target frequency   03:05

3   or describe a target frequency, correct?   03:05

4   A.   Varying about a target -- that's correct.   03:05

5   Q.   The remaining portion of the preamble, you   03:05

6   agree that the Wang reference would satisfy, correct?   03:05

7   A.   I believe so.   03:05

8   Q.   Okay. And I'm going to give you what will be   03:05

9   marked as Blauschild Exhibit 13, which is a copy of a   03:06

10   document bearing production numbers FCS1692016 through   03:06

11   1692043. It's also marked as DX 10.   03:06

12   03:06

13   (Defendants' Exhibit 13 was marked.)   03:06

14   03:06

15   THE WITNESS: Should I -- can I fold this one   03:06

16   up?   03:06

17   MR. DE BLANK: 03:06

18   Q.   You can set that aside for now.   03:06

19   A.   Okay.   03:06

20   MR. POLLACK: Just for the record, this one   03:06

21   also has two copies of the -- actually I think this one   03:06

22   has three copies of the article.   03:06

23   THE WITNESS: I didn't get it, right? It's a   03:06

24   little thick.   03:06

25

EXHIBIT 6

® POWER INTEGRATIONS, INC.

TNY264/266-268
TinySwitch-II Family

Enhanced, Energy Efficient, Low Power Off-line Switcher

Product Highlights

TinySwitch-II Features Reduce System Cost

- Fully integrated auto-restart for short circuit and open loop fault protection–saves external component costs
- Built-in circuitry practically eliminates audible noise with ordinary varnished transformer
- Programmable line under-voltage detect feature prevents power on/off glitches–saves external components
- Frequency jittering dramatically reduces EMI (~10 dB) –minimizes EMI filter component costs
- 132 kHz operation reduces transformer size–allows use of EF12.6 or EE13 cores for low cost and small size
- Very tight tolerances and negligible temperature variation on key parameters eases design and lowers cost
- Lowest component count switcher solution

Better Cost/Performance over RCC & Linears

- Lower system cost than RCC, discrete PWM and other integrated/hybrid solutions
- Cost effective replacement for bulky regulated linears
- Simple ON/OFF control–no loop compensation needed
- No bias winding–simpler, lower cost transformer

EcoSmart®–Extremely Energy Efficient

- No load consumption < 50 mW with bias winding and < 250 mW without bias winding at 265 VAC input
- Meets Blue Angel, Energy Star, and EC requirements
- Ideal for cell-phone charger and PC standby applications

High Performance at Low Cost

- High voltage powered–ideal for charger applications
- High bandwidth provides fast turn on with no overshoot
- Current limit operation rejects line frequency ripple
- Built-in current limit and thermal protection

Description

TinySwitch-II maintains the simplicity of the TinySwitch topology, while providing a number of new enhancements to further reduce system cost and component count, and to practically eliminate audible noise. Like TinySwitch, a 700 V power MOSFET, oscillator, high voltage switched current source, current limit and thermal shutdown circuitry are integrated onto a monolithic device. The start-up and operating power are derived directly from the voltage on the DRAIN pin, eliminating the need for a bias winding and associated circuitry. In addition, the
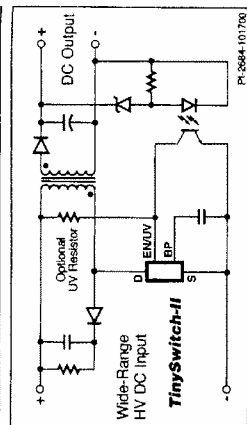
Figure 1. Typical Standby Application.

OUTPUT POWER TABLE

PRODUCT[3]	230 VAC ±15%		85-265 VAC	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
TNY264P or G	5.5 W	9 W	4 W	6 W
TNY266P or G	10 W	15 W	6 W	9.5 W
TNY267P or G	13 W	19 W	8 W	12 W
TNY268P or G	16 W	23 W	10 W	15 W

Table 1. Notes: 1. Typical continuous power in a non-ventilated enclosed adapter measured at 50 °C ambient. 2. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at 50 °C ambient. (See key applications section for details). 3. Packages: P: DIP-8B, G: SMD-8B. Please see ordering information.

TinySwitch-II devices incorporate auto-restart, line under-voltage sense, and frequency jittering. An innovative design minimizes audio frequency components in the simple ON/OFF control scheme to practically eliminate audible noise with standard taped/varnished transformer construction. The fully integrated auto-restart circuit safely limits output power during fault conditions such as output short circuit or open loop, reducing component count and secondary feedback circuitry cost. An optional line under-voltage threshold, which eliminates power down glitches caused by the slow discharge of input storage capacitors present in applications such as standby supplies. The operating frequency of 132 kHz is jittered to significantly reduce both the quasi-peak and average EMI, minimizing filtering cost.

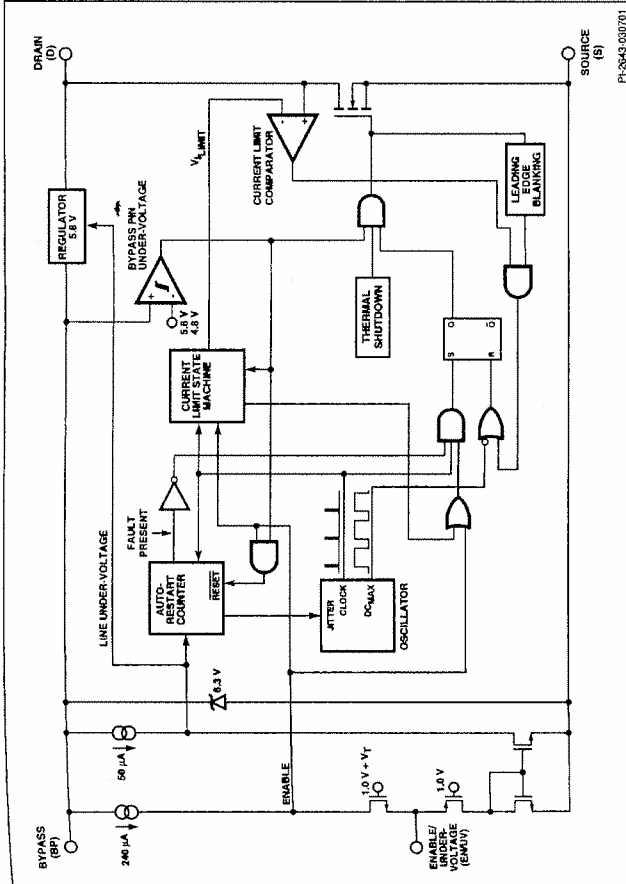Figure 2. Functional Block Diagram.

Figure 3. Pin Configuration.

Pin Functional Description

DRAIN (D) Pin:
Power MOSFET drain connection. Provides internal operating current for both start-up and steady-state operation.

BYPASS (BP) Pin:
Connection point for a 0.1 µF external bypass capacitor for the internally generated 5.8 V supply.

ENABLE/UNDER-VOLTAGE (EN/UV) Pin:
This pin has dual functions: enable input and line under-voltage sense. During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is terminated when a current greater than 240 µA is drawn from this pin. This pin also senses line under-voltage conditions through an external resistor connected to the DC line voltage. If there is no external resistor connected to this pin, TinySwitch-II detects its absence and disables the line under-voltage function.

SOURCE (S) Pin:
Control circuit common, internally connected to output MOSFET source.

SOURCE (HV RTN) Pin:
Output MOSFET source connection for high voltage return.

2-62

2-63

B 701

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TinySwitch-II Functional Description

TinySwitch-II combines a high voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (Pulse Width Modulator) controllers, TinySwitch-II uses a simple ON/OFF control to regulate the output voltage.

The TinySwitch-II controller consists of an Oscillator, Enable Circuit (Sense and Logic), Current Limit State Machine, 5.8 V Regulator, Bypass pin Under-Voltage Circuit, Over Temperature Protection, Current Limit Circuit, Leading Edge Blanking and a 700 V power MOSFET. TinySwitch-II incorporates additional circuitry for Line Under-Voltage Sense, Auto-Restart and Frequency Jitter. Figure 2 shows the functional block diagram with the most important features.

Oscillator

The typical oscillator frequency is internally set to an average of 132 kHz. Two signals are generated from the oscillator: the Maximum Duty Cycle signal (DC_{MAX}) and the Clock signal that indicates the beginning of each cycle.

The TinySwitch-II oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 8 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 4 illustrates the frequency jitter of the TinySwitch-II.

Enable Input and Current Limit State Machine

The enable input circuit at the EN/UV pin consists of a low impedance source follower output set at 1.0 V. The current through the source follower is limited to 240 μA. When the current out of this pin exceeds 240 μA, a low logic level
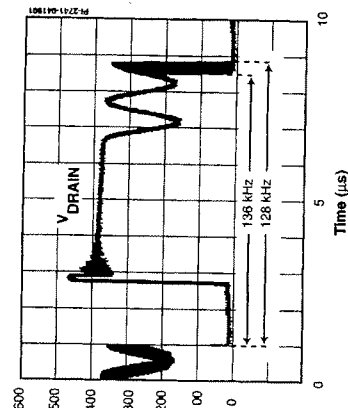
Figure 4. Frequency Jitter.

(disable) is generated at the output of the enable circuit. This enable circuit output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled). If low, the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the EN/UV pin voltage or current during the remainder of the cycle are ignored.

The Current Limit State Machine reduces the current limit by discrete amounts at light loads when TinySwitch-II is likely to switch in the audible frequency range. The lower current limit raises the effective switching frequency above the audio range and reduces the transformer flux density including the associated audible noise. The state machine monitors the sequence of EN/UV pin voltage levels to determine the load condition and adjusts the current limit level accordingly in discrete amounts.

Under most operating conditions (except when close to no-load), the low impedance of the source follower keeps the voltage on the EN/UV pin from going much below 1.0 V in the disabled state. This improves the response time of the optocoupler that is usually connected to this pin.

5.8 V Regulator and 6.3 V Shunt Voltage Clamp

The 5.8 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.8 V by drawing a current from the voltage on the DRAIN pin, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node for the TinySwitch-II. When the MOSFET is on, the TinySwitch-II operates from the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows TinySwitch-II to operate continuously from current it takes from the DRAIN pin. A bypass capacitor value of 0.1 μF is sufficient for both high frequency decoupling and energy storage.

In addition, there is a 6.3 V shunt regulator clamping the BYPASS pin at 6.3 V when current is provided to the BYPASS pin through an external resistor. This facilitates powering of TinySwitch-II externally through a bias winding to decrease the no load consumption to about 50 mW.

BYPASS Pin Under-Voltage

The BYPASS pin under-voltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below 4.8 V. Once the BYPASS pin voltage drops below 4.8 V, it must rise back to 5.8 V to enable (turn-on) the power MOSFET.

Over Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is typically set at 135 °C with 70 °C hysteresis. When the die temperature rises above this threshold the power MOSFET is disabled and remains disabled until the die temperature falls by 70 °C, at which point it is re-enabled. A large hysteresis of 70 °C (typical) is provided to prevent overheating of the PC board due to a continuous fault condition.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The current limit state machine reduces the current limit threshold by discrete amounts under medium and light loads.

The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

Auto-Restart

In the event of a fault condition such as output overload, output short circuit, or an open loop condition, TinySwitch-II enters into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the EN/UV pin is pulled low. If the EN/UV pin is not pulled low for 50 ms, the power MOSFET switching is normally disabled for 850 ms (except in the case of line under-voltage condition in which case it is disabled until the condition is removed). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. Figure 5 illustrates auto-restart circuit operation in the presence of an output short circuit.

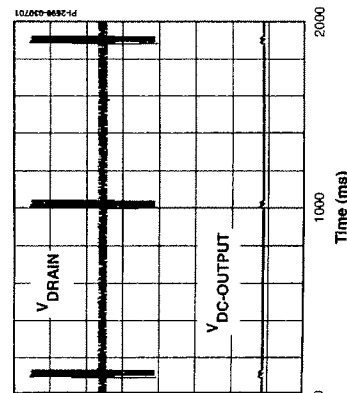In the event of a line under-voltage condition, the switching of

Figure 5. TinySwitch-II Auto-Restart Operation.

the power MOSFET is disabled beyond its normal 850 ms time until the line under-voltage condition ends.

Line Under-Voltage Sense Circuit

The DC line voltage can be monitored by connecting an external resistor from the DC line to the EN/UV pin. During power-up or when the switching of the power MOSFET is disabled in auto-restart, the current into the EN/UV pin must exceed 50 μA to initiate switching of the power MOSFET. During power-up, this is implemented by holding the BYPASS pin to 4.8 V while the line under-voltage condition exists. The BYPASS pin then rises from 4.8 V to 5.8 V when the line under-voltage condition goes away. When the switching of the power MOSFET is disabled in auto-restart mode and a line under-voltage condition exists, the auto-restart counter is stopped. This stretches the disable time beyond its normal 850 ms until the line under-voltage condition ends.

The line under-voltage circuit also detects when there is no external resistor connected to the EN/UV pin (less than ~ 2 μA into pin). In this case the line under-voltage function is disabled.

TinySwitch-II Operation

TinySwitch-II devices operate in the current limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the DC_{MAX} limit is reached. As the highest current limit level and frequency of a TinySwitch-II design are constant, the power delivered to the load is proportional to the primary inductance of the transformer and peak primary current squared. Hence, designing the supply involves calculating the primary inductance of the transformer for the maximum output power required. If the TinySwitch-II is appropriately chosen for the power level, the current in the calculated inductance will ramp up to current limit before the DC_{MAX} limit is reached.

Enable Function

TinySwitch-II senses the EN/UV pin to determine whether or not to proceed with the next switch cycle as described earlier. The sequence of cycles is used to determine the current limit. Once a cycle is started, it always completes the cycle (even when the EN/UV pin changes state half way through the cycle). This operation results in a power supply in which the output voltage ripple is determined by the output capacitor, amount of energy per switch cycle and the delay of the feedback.

The EN/UV pin signal is generated on the secondary by comparing the power supply output voltage with a reference voltage. The EN/UV pin signal is high when the power supply output voltage is less than the reference voltage.

In a typical implementation, the EN/UV pin is driven by an optocoupler. The collector of the optocoupler transistor is connected to the EN/UV pin and the emitter is connected to
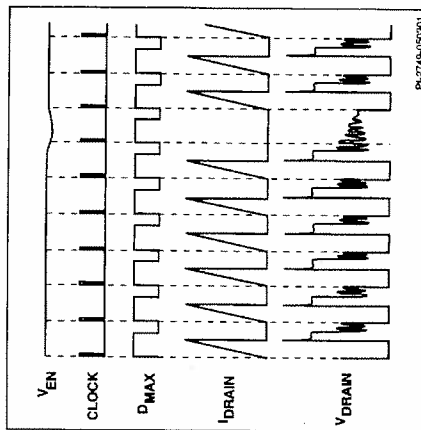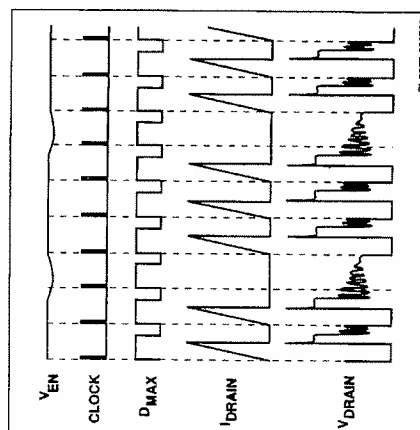
TNY264/266-268

the SOURCE pin. The optocoupler LED is connected in series with a Zener diode across the DC output voltage to be regulated. When the output voltage exceeds the target regulation voltage level (optocoupler LED voltage drop plus Zener voltage), the optocoupler LED will start to conduct, pulling the EN/UV pin low. The Zener diode can be replaced by a TL431 reference circuit for improved accuracy.

ON/OFF Operation with Current Limit State Machine
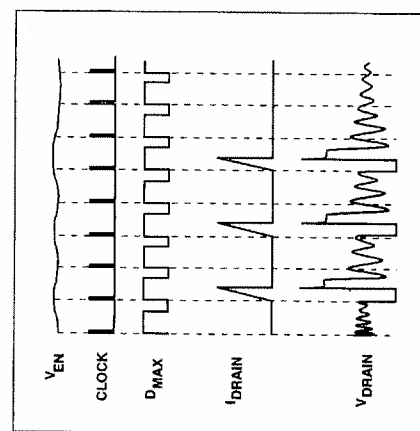The internal clock of the TinySwitch-II runs all the time. At the beginning of each clock cycle, it samples the EN/UV pin to decide whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, when the EN/UV pin is high (less than 240 µA out of the pin), a switching cycle with the full current limit occurs. At lighter loads, when EN/UV is high, a switching cycle with a reduced current limit occurs.

At near maximum load, TinySwitch-II will conduct during nearly all of its clock cycles (Figure 6). At slightly lower load, it will "skip" additional cycles in order to maintain voltage regulation at the power supply output (Figure 7). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 8). At very light loads, the current limit will be reduced even further (Figure 9). Only a small percentage of cycles will occur to satisfy the power consumption of the power supply.

The response time of the TinySwitch-II ON/OFF control scheme is very fast compared to normal PWM control. This provides tight regulation and excellent transient response.

Power Up/Down
The TinySwitch-II requires only a 0.1 µF capacitor on the BYPASS pin. Because of its small size, the time to charge this capacitor is kept to an absolute minimum, typically 0.6 ms. Due to the fast nature of the ON/OFF feedback, there is no overshoot at the power supply output. When an external resistor (2 MΩ) is connected from the positive DC input to the EN/UV pin, the power MOSFET switching will be delayed during power-up until the DC line voltage exceeds the threshold (100 V). Figures 10 and 11 show the power-up timing waveform of TinySwitch-II in applications with and without an external resistor (2 MΩ) connected to the EN/UV pin.

During power-down, when an external resistor is used, the power MOSFET will switch for 50 ms after the output loses regulation. The power MOSFET will then remain off without any glitches since the under-voltage function prohibits restart when the line voltage is low.

Figure 12 illustrates a typical power-down timing waveform of TinySwitch-II. Figure 13 illustrates a very slow power-down timing waveform of TinySwitch-II as in standby applications. The external resistor (2 MΩ) is connected to the EN/UV pin in this case to prevent unwanted restarts.

Figure 6. TinySwitch-II Operation at Near Maximum Loading.

Figure 7. TinySwitch-II Operation at Moderately Heavy Loading.

Figure 8. TinySwitch-II Operation at Medium Loading.

Figure 9. TinySwitch-II Operation at Very Light Load.

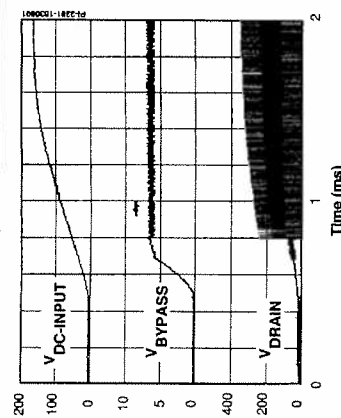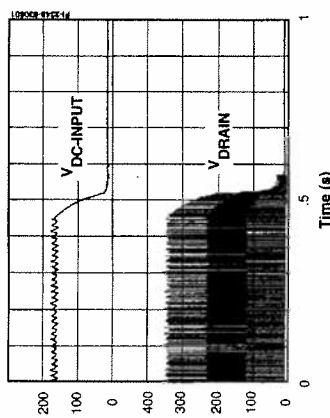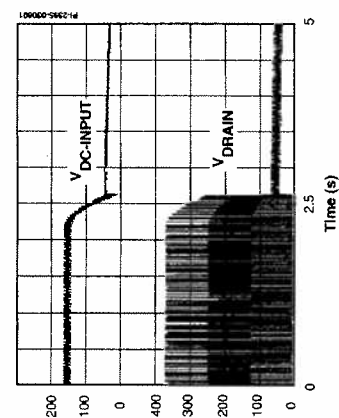Figure 10. TinySwitch-II Power-up with Optional External UV Resistor (2 MΩ) Connected to EN/UV Pin.

Figure 11. TinySwitch-II Power-up without Optional External UV Resistor Connected to EN/UV Pin.

Figure 12. Normal Power-down Timing (without UV).

Figure 13. Slow Power-down Timing with Optional External (2 MΩ) UV Resistor Connected to EN/UV Pin.

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The TinySwitch-II does not require a bias winding to provide power to the chip, because it draws the power directly from the DRAIN pin (see Functional Description above). This has two main benefits. First, for a nominal application, this eliminates the cost of a bias winding and associated components. Secondly, for battery charger applications, the current-voltage characteristic often allows the output voltage to fall close to zero volts while still delivering power. This type of application normally requires a forward-bias winding which has many more associated components. With TinySwitch-II, neither are necessary. For applications that require a very low no-load power consumption (50 mW), a resistor from a bias winding to the BYPASS pin can provide the power to the chip. The minimum recommended current supplied is 750 μA. The BYPASS pin in this case will be clamped at 6.3 V. This method will eliminate the power draw from the DRAIN pin, thereby reducing the no-load power consumption and improving full-load efficiency.

Current Limit Operation
Each switching cycle is terminated when the DRAIN current reaches the current limit of the TinySwitch-II. Current limit operation provides good line ripple rejection and relatively constant power delivery independent of input voltage.

BYPASS Pin Capacitor
The BYPASS pin uses a small 0.1 μF ceramic capacitor for decoupling the internal power supply of the TinySwitch-II.
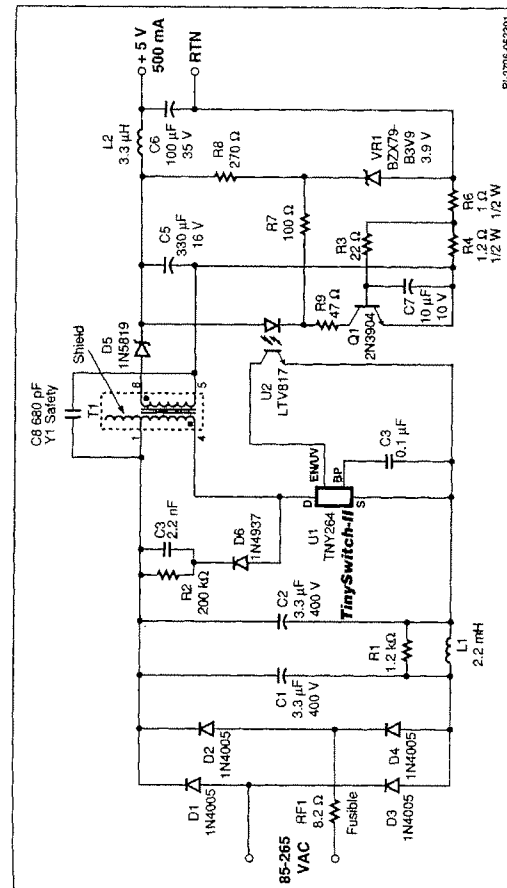
Figure 14. 2.5 W Constant Voltage, Constant Current Battery Charger with Universal Input (85-265 VAC).

Application Examples

The TinySwitch-II is ideal for low cost, high efficiency power supplies in a wide range of applications such as cellular phone chargers, PC standby, TV standby, AC adapters, motor control, appliance control and ISDN or a DSL network termination. The 132 kHz operation allows the use of a low cost EE13 or EF12.6 core transformer while still providing good efficiency. The frequency jitter in TinySwitch-II makes it possible to use a single inductor (or two small resistors for under 3 W applications if lower efficiency is acceptable) in conjunction with two input capacitors for input EMI filtering. The auto-restart function removes the need to oversize the output diode for short circuit conditions allowing the design to be optimized for low cost and maximum efficiency. In charger applications, it eliminates the need for a second optocoupler and Zener diode for open loop fault protection. Auto-restart also saves the cost of adding a fuse or increasing the power rating of the current sense resistors to survive reverse battery conditions. For applications requiring under-voltage lock out (UVLO), such as PC standby, the TinySwitch-II eliminates several components and saves cost. TinySwitch-II is well suited for applications that require constant voltage and constant current output. As TinySwitch-II is always powered from the input high voltage, it therefore does not rely on bias winding voltage. Consequently this greatly simplifies designing chargers that must work down to zero volts on the output.

2.5 W CV/CC Cell-Phone Charger
As an example, Figure 14 shows a TNY264 based 5 V, 0.5 A, cellular phone charger operating over a universal input range (85-265 VAC). The inductor (L1) forms a π-filter in conjunction with C1 and C2. The resistor R1 damps resonances in the inductor L1. Frequency jittering operation of TinySwitch-II allows the use of a simple π-filter described above in combination with a single low value Y1-capacitor (C8) to meet worldwide conducted EMI standards. The addition of a shield winding in the transformer allows conducted EMI to be met even with the output capacitively earthed (which is the worst case condition for EMI). The diode D6, capacitor C3 and resistor R2 comprise the clamp circuit, limiting the leakage inductance turn-off voltage spike on the TinySwitch-II DRAIN pin to a safe value. The output voltage is determined by the sum of the optocoupler U2 LED forward drop (~1 V), and Zener diode VR1 voltage. Resistor R8 maintains a bias current through the Zener diode to ensure it is operated close to the Zener test current.

A simple constant current circuit is implemented using the V_{BE} of transistor Q1 to sense the voltage across the current sense resistor R4. When the drop across R4 exceeds the V_{BE} of transistor Q1, it turns on and takes over control of the loop by driving the optocoupler LED. Resistor R6 assures sufficient voltage to keep the control loop in operation down to zero volts at the output. With the output shorted, the drop across R4 and R6 (~1.2 V) is sufficient to keep the Q1 and LED circuit active. Resistors R7 and R9 limit the forward current that could be drawn through VR1 by Q1 under output short circuit conditions, due to the voltage drop across R4 and R6.

Capacitor C1 provides high frequency decoupling of the high voltage DC supply, only necessary if there is a long trace length from the DC bulk capacitors of the main supply. The line sense resistors R2 and R3 sense the DC input voltage for line under-voltage. When the AC is turned off, the under-voltage detect feature of the TinySwitch-II prevents auto-restart glitches at the output caused by the slow discharge of large storage capacitance in the main converter. This is achieved by preventing the TinySwitch-II from switching when the input voltage goes below a level needed to maintain output regulation, and keeping it off until the input voltage goes above the under-voltage threshold, when the AC is turned on again. With R2 and R3, giving a combined value of 4 MΩ, the power up under-voltage threshold is set at 200 VDC, slightly below the lowest required operating DC input voltage, for start-up at 170 VAC, with doubler. This feature saves several components needed to implement the glitch-free turn-off compared with discrete or TOPSwitch-II based designs. During turn-on the rectified DC input voltage needs to exceed 200 V under-voltage threshold for the power supply to start operation. But, once the power supply is on it will continue to operate down to 140 V rectified DC input voltage to provide the required hold up time for the standby output.

10 and 15 W PC Standby Circuits
Figures 15 and 16 show examples of circuits for PC standby applications. They both provide two outputs: an isolated 5 V and a 12 V primary-referenced output. The first, using TNY266P, provides 10 W, and the second, using TNY267P, 15 W of output power. Both operate from an input range of 140 to 375 VDC, corresponding to a 230 VAC or 100/115 VAC with doubler input. The designs take advantage of the line under-voltage detect, auto-restart and higher switching frequency of TinySwitch-II. Operation at 132 kHz allows the use of a smaller and lower cost transformer core, EE16 for 10 W and EE22 for 15 W. The removal of pin 6 from the 8 pin DIP TinySwitch-II packages provides a large creepage distance which improves reliability in high pollution environments such as fan cooled PC power supplies.

The auxiliary primary side winding is rectified and filtered by D2 and C2 to create a 12 V primary bias output voltage for the main power supply primary controller. In addition, this voltage is used to power the TinySwitch-II externally, supplying the TinySwitch-II via R4. Although not necessary for operation, supplying the TinySwitch-II externally reduces the device quiescent dissipation by disabling the internal drain derived current source normally used to keep the BYPASS pin capacitor (C3) charged. An R4 value of 10 kΩ provides 600 μA into the BYPASS pin, which is slightly in excess of the current consumption of TinySwitch-II. The excess current is safely clamped by an on-chip active Zener diode to 6.3 V.

The secondary winding is rectified and filtered by D3 and C6. For a 15 W design an additional output capacitor, C7, is required due to the larger secondary ripple currents compared to the 10 W PC standby design. The auto-restart function limits output current during short circuit conditions, removing the need to over rate D3. Switching noise filtering is provided by L1 and C8. The 5 V output is sensed by U2 and VR1. R5 is used to ensure that the Zener diode is biased at its test current.

The Zener regulation method provides sufficient accuracy (typ. ± 3%). This is possible because TinySwitch-II limits the dynamic range of the optocoupler LED current, allowing the Zener diode to operate at near constant bias current.

TNY264/266-268

Key Application Considerations

TinySwitch-II vs. TinySwitch

Table 2 compares the features and performance differences between the TNY254 device of the TinySwitch family with the TinySwitch-II family of devices. Many of the new features eliminate the need for or reduce the cost of circuit components. Other features simplify the design and enhance performance.

	TinySwitch	TinySwitch-II	Benefit
Switching Frequency and Tolerance Temperature Variation (0 - 100 °C)**	44 kHz ±10% (@25 °C) +8%	132 kHz ±6% (@25 °C) +2%	• Smaller transformer for low cost • Ease of design • Manufacturability • Optimum design for lower cost
Active Frequency Jitter	N/A*	±4 kHz	• Lower EMI minimizing filter component costs
Transformer Audible Noise Reduction	N/A*	Yes - built into controller	• Practically eliminates audible noise with ordinary dip varnished transformer -- no special construction or gluing required
Line UV Detect	N/A*	Single resistor programmable	• Prevents power on/off glitches
Current Limit Tolerance Temperature Variation (0 - 100 °C)**	± 11% (@25 °C) -8%	± 7% (@25 °C) 0%	• Increases power capability and simplifies design for high volume manufacturing
Auto-Restart	N/A*	6% effective on-time	• Limits output short-circuit current to less than full load current - No output diode size penalty. • Protects load in open loop fault conditions - No additional components required
BYPASS Pin Zener Clamp	N/A*	Internally clamped to 6.3 V	• Allows TinySwitch-II to be powered from a low voltage bias winding to improve efficiency and to reduce on-chip power dissipation
DRAIN Creepage at Package	0.037" / 0.94 mm	0.137" / 3.48 mm	• Greater immunity to arcing as a result of dust, debris or other contaminants build-up

*Not available.   ** See typical performance curves.

Table 2. Comparison Between TinySwitch and TinySwitch-II.

Design

Output Power

Table 1 (front page) shows the practical maximum continuous output power levels that can be obtained under the following conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, or 240 V or higher for 230 VAC input or 115 VAC input with a voltage doubler. This corresponds to a filter capacitor of 3 μF/W for universal input and 1 μF/W for 230 or 115 VAC with doubler input.

TNY264/266-268

PERFORMANCE SUMMARY
Continuous Output Power: 10.24 W
Efficiency: ≥ 75%

Figure 15. 10 W PC Standby Supply.

PERFORMANCE SUMMARY
Continuous Output Power: 15.24 W
Efficiency: ≥ 78%

Figure 16. 15 W PC Standby Supply.

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2-71

PIF 56299

TNY264/266-268

Figure 17. Recommended Circuit Board Layout for TinySwitch-II with Under-Voltage Lock Out Resistor.

should be taken directly from the secondary winding pin and not from the Y-capacitor connection point.

PC Board Cleaning
Power Integrations does not recommend the use of "no clean" flux.

For the most up-to-date information visit the PI Web site at: www.powerint.com

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2. A secondary output of 5 V with a Schottky rectifier diode.

3. Assumed efficiency of 77% (TNY267 & TNY268), 75% (TNY266) and 73% (TNY264).

4. The parts are board mounted with SOURCE pins soldered to sufficient area of copper to keep the die temperature at or below 100 °C.

In addition to the thermal environment (sealed enclosure, ventilated, open frame, etc.), the maximum power capability of TinySwitch-II in a given application depends on transformer core size and design (continuous or discontinuous), efficiency, minimum specified input voltage, input storage capacitance, output voltage, output diode forward drop, etc., and can be different from the values shown in Table 1.

Audible Noise
The TinySwitch-II practically eliminates any transformer audio noise using simple ordinary varnished transformer construction. No gluing of the cores is needed. The audio noise reduction is accomplished by the TinySwitch-II controller reducing the current limit in discrete steps as the load is reduced. This minimizes the flux density in the transformer when switching at audio frequencies.

Worst Case EMI & Efficiency Measurement
Since identical TinySwitch-II supplies may operate at several different frequencies under the same load and line conditions, care must be taken to ensure that measurements are made under worst case conditions. When measuring efficiency or EMI verify that the TinySwitch-II is operating at maximum frequency and that measurements are made at both low and high line input voltages to ensure the worst case result is obtained.

Layout

Single Point Grounding
Use a single point ground connection at the SOURCE pin for the BYPASS pin capacitor and the Input Filter Capacitor (see Figure 17).

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and TinySwitch-II together should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp (as shown in Figure 14). A Zener and diode clamp (200 V) across the primary or a single 550 V Zener clamp from DRAIN to SOURCE can also be used. In all cases care should be taken to minimize the circuit path from the clamp components to the transformer and TinySwitch-II.

Thermal Considerations
Copper underneath the TinySwitch-II acts not only as a single point ground, but also as a heatsink. The hatched areas shown in Figure 17 should be maximized for good heat sinking of TinySwitch-II and the same applies to the output diode.

EN/UV pin
If a line under-voltage detect resistor is used then the resistor should be mounted as close as possible to the EN/UV pin to minimize noise pick up.

The voltage rating of a resistor should be considered for the under-voltage detect (Figure 15: R2, R3) resistors. For 1/4 W resistors, the voltage rating is typically 200 V continuous, whereas for 1/2 W resistors the rating is typically 400 V continuous.

Y-Capacitor
The placement of the Y-capacitor should be directly from the primary bulk capacitor positive rail to the common/return terminal on the secondary side. Such placement will maximize the EMI benefit of the Y-capacitor and avoid problems in common-mode surge testing.

Optocoupler
It is important to maintain the minimum circuit path from the optocoupler transistor to the TinySwitch-II EN/UV and SOURCE pins to minimize noise coupling.

The EN/UV pin connection to the optocoupler should be kept to an absolute minimum (less than 12.7 mm or 0.5 in.), and this connection should be kept away from the DRAIN pin (minimum of 5.1 mm or 0.2 in.).

Output Diode
For best performance, the area of the loop connecting the secondary winding, the Output Diode and the Output Filter Capacitor, should be minimized. See Figure 17 for optimized layout. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for adequate heatsinking.

Input and Output Filter Capacitors
There are constrictions in the traces connected to the input and output filter capacitors. These constrictions are present for two reasons. The first is to force all the high frequency currents to flow through the capacitor (if the trace were wide then it could flow around the capacitor). Secondly, the constrictions minimize the heat transferred from the TinySwitch-II to the input filter capacitor and from the secondary diode to the output filter capacitor. The common/return (the negative output terminal in Figure 17) terminal of the output filter capacitor should be connected with a short, low impedance path to the secondary winding. In addition, the common/return output connection
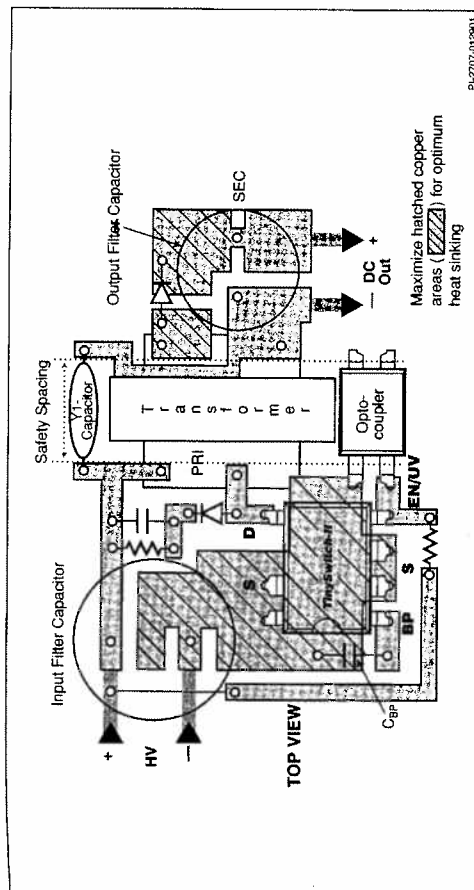
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CONTROL FUNCTIONS (cont)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
		SOURCE = 0 V; T$_J$ = -40 to 125 °C, See Figure 18 (Unless Otherwise Specified)				
EN/UV Pin Line Under-voltage Threshold	I$_{UV}$	T$_J$ = 25 °C	44	49	54	µA

CIRCUIT PROTECTION

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Current Limit	I$_{LIMIT}$	TNY264 T$_J$ = 25 °C, di/dt = 50 mA/µs, See Note E	233	250	267	mA
		TNY266 T$_J$ = 25 °C, di/dt = 70 mA/µs, See Note E	325	350	375	
		TNY267 T$_J$ = 25 °C, di/dt = 90 mA/µs, See Note E	419	450	481	
		TNY268 T$_J$ = 25 °C, di/dt = 110 mA/µs, See Note E	512	550	588	
Initial Current Limit	I$_{INIT}$	See Figure 21, T$_J$ = 25 °C	0.65 x I$_{LIMIT (MIN)}$			mA
Leading Edge Blanking Time	t$_{LEB}$	T$_J$ = 25 °C, See Note F	170	215		ns
Current Limit Delay	t$_{ILD}$	T$_J$ = 25 °C, See Note F, G		150		ns
Thermal Shutdown Temperature			125	135	150	°C
Thermal Shutdown Hysteresis				70		°C

OUTPUT

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ON-State Resistance	R$_{DS(ON)}$	TNY264 T$_J$ = 25 °C, I$_D$ = 25 mA		28	32	Ω
		T$_J$ = 100 °C		42	48	
		TNY266 I$_D$ = 35 mA, T$_J$ = 25 °C		14	16	
		T$_J$ = 100 °C		21	24	
		TNY267 I$_D$ = 45 mA, T$_J$ = 25 °C		7.8	9.0	
		T$_J$ = 100 °C		11.7	13.5	
		TNY268 I$_D$ = 55 mA, T$_J$ = 25 °C		5.2	6.0	
		T$_J$ = 100 °C		7.8	9.0	
OFF-State Leakage	I$_{DSS}$	V$_{BP}$ = 6.2 V, V$_{EN/UV}$ = 0 V, V$_{DS}$ = 560 V, T$_J$ = 125 °C, TNY264 TNY266			50	µA
		TNY267 TNY268			100	

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ABSOLUTE MAXIMUM RATINGS[1]

DRAIN Voltage .... -0.3 V to 700 V
Peak DRAIN Current (TNY264) .... 400 mA
Peak DRAIN Current (TNY266) .... 560 mA
Peak DRAIN Current (TNY267) .... 720 mA
Peak DRAIN Current (TNY268) .... 880 mA
EN/UV Voltage .... -0.3 V to 9 V
EN/UV Current .... 100 mA
BYPASS Voltage .... -0.3 V to 9 V
Storage Temperature .... -65 to 150 °C
Operating Junction Temperature[2] .... -40 to 150 °C
Lead Temperature[3] .... 260 °C

Notes:
1. All voltages referenced to SOURCE, T$_A$ = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

THERMAL IMPEDANCE

Thermal Impedance: P/G Package:
(θ$_{JA}$) .... 45 °C/W[2]; 35 °C/W[3]
(θ$_{JC}$)[4] ...... 11 °C/W

Notes:
1. Measured on the SOURCE pin close to plastic interface.
2. Soldered to 0.36 sq. inch (232 mm²), 2oz. (610 gm/m²) copper clad.
3. Soldered to 1 sq. inch (645 mm²), 2oz. (610 gm/m²) copper clad.

CONTROL FUNCTIONS

Parameter	Symbol	Conditions		Min	Typ	Max	Units
		SOURCE = 0 V; T$_J$ = -40 to 125 °C, See Figure 18 (Unless Otherwise Specified)					
Output Frequency	f$_{OSC}$	T$_J$ = 25 °C, See Figure 4	Average	124	132	140	kHz
			Peak-Peak Jitter		8		%
Maximum Duty Cycle	DC$_{MAX}$	S1 Open		62	65	68	%
EN/UV Pin Turnoff Threshold Current	I$_{DIS}$	T$_J$ = -40 °C to 125 °C		-300	-240	-170	µA
EN/UV Pin Voltage	V$_{EN}$	I$_{EN/UV}$ = -125 µA		0.4	1.0	1.5	V
		I$_{EN/UV}$ = 25 µA		1.3	2.3	2.7	
	I$_{S1}$	V$_{EN/UV}$ = 0 V		320	430	500	µA
DRAIN Supply Current	I$_{S2}$	EN/UV Open (MOSFET Switching) See Note A, B	TNY264	170	225	270	µA
			TNY266	200	265	320	
			TNY267	240	315	380	
			TNY268	285	380	460	
BYPASS Pin Charge Current	I$_{CH1}$	V$_{BP}$ = 0 V, T$_J$ = 25 °C, See Note C, D	TNY264	-5.5	-3.3	-1.8	mA
			TNY266-268	-7.5	-4.6	-2.5	
	I$_{CH2}$	V$_{BP}$ = 4 V, T$_J$ = 25 °C, See Note C, D	TNY264	-3.8	-2.0	-1.0	
			TNY266-268	-4.5	-3.0	-1.5	
BYPASS Pin Voltage	V$_{BP}$	See Note C		5.6	5.85	6.15	V
BYPASS Pin Voltage Hysteresis	V$_{BPH}$			0.80	0.95	1.20	V

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Figure 18. TinySwitch-II General Test Circuit.
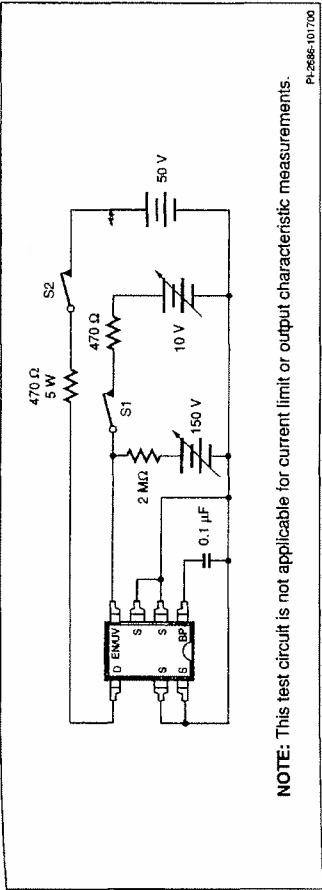
NOTE: This test circuit is not applicable for current limit or output characteristic measurements.

Figure 19. TinySwitch-II Duty Cycle Measurement.
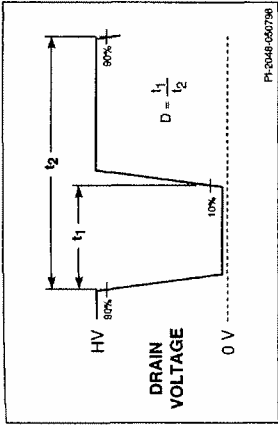
$$D = \frac{t_1}{t_2}$$
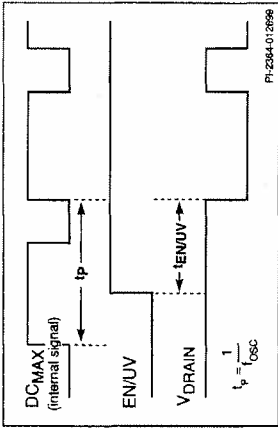
Figure 20. TinySwitch-II Output Enable Timing.

$$t_P = \frac{1}{f_{OSC}}$$
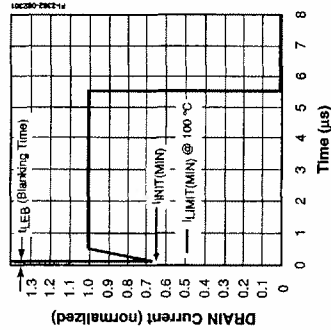
Figure 21. Current Limit Envelope.

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Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 18 (Unless Otherwise Specified)	Min	Typ	Max	Units
OUTPUT (cont.)						
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, $V_{EN/UV}$ = 0 V, I_{DS} = 100 µA, T_J = 25 °C	700			V
Rise Time	t_R	Measured in a Typical Flyback		50		ns
Fall Time	t_F	Converter Application		50		ns
Drain Supply Voltage			50			V
Output EN/UV Delay	$t_{EN/UV}$	See Figure 20			10	µs
Output Disable Setup Time	t_{DST}			0.5		µs
Auto-Restart ON-Time	t_{AR}	T_J = 25 °C See Note H		50		ms
Auto-Restart Duty Cycle	DC_{AR}			5.6		%

NOTES:

A. Total current consumption is the sum of I_{S1} and I_{DSS} when EN/UV pin is shorted to ground (MOSFET not switching) and the sum of I_{S2} and I_{DSS} when EN/UV pin is open (MOSFET switching).

B   Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BYPASS pin current at 6.1 V.

C. BYPASS pin is not intended for sourcing supply current to external circuitry.

D. See typical performance characteristics section for BYPASS pin start-up charging waveform.

E. For current limit at other di/dt values, refer to Figure 25.

F. This parameter is derived from characterization.

G. This parameter is derived from the change in current limit measured at 1X and 4X of the di/dt shown in the I_{LIMIT} specification.

H. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency).

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Typical Performance Characteristics (cont.)

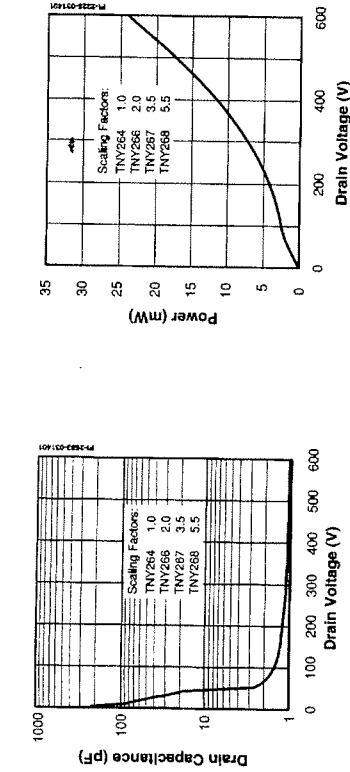Figure 28. C_{oss} vs. Drain Voltage.

Figure 29. Drain Capacitance Power.
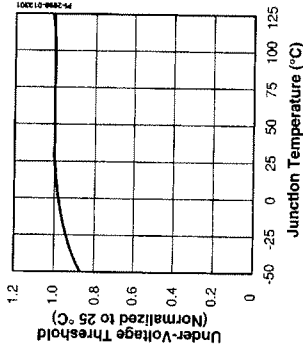
Figure 30. Undervoltage Threshold vs. Temperature.

TinySwitch Product Family		
Series Number		
Package Identifier		
	G	Plastic Surface Mount DIP
	P	Plastic DIP
Package/Lead Options		
	Blank	Standard Configurations
	TL	Tape & Reel, 1 k pcs minimum, G Package only

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Typical Performance Characteristics
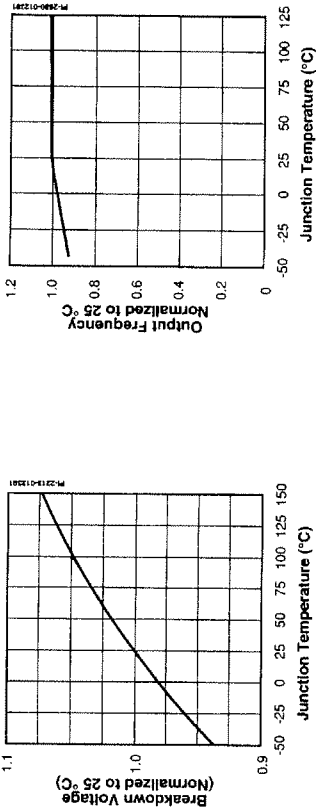
Figure 22. Breakdown vs. Temperature.
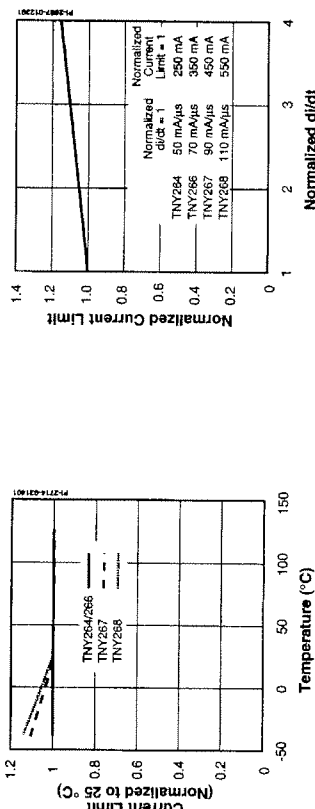
Figure 23. Frequency vs. Temperature.
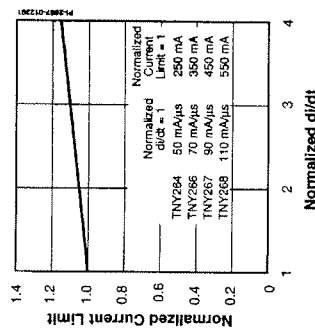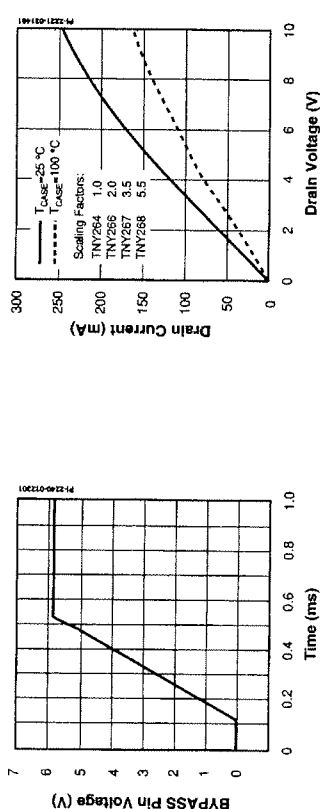
Figure 24. Current Limit vs. Temperature.
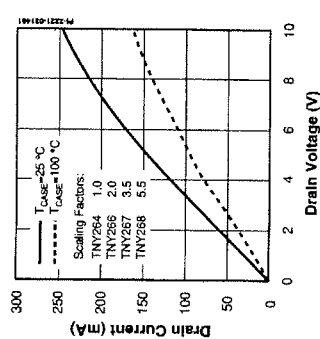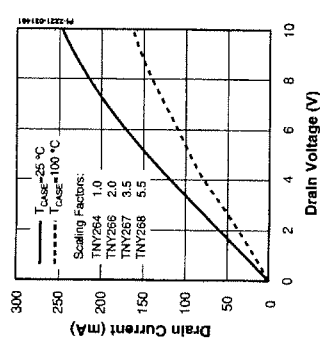
Figure 25. Current Limit vs. di/dt.

Figure 26. Bypass Pin Start-up Waveform.

Figure 27. Output Characteristic.

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